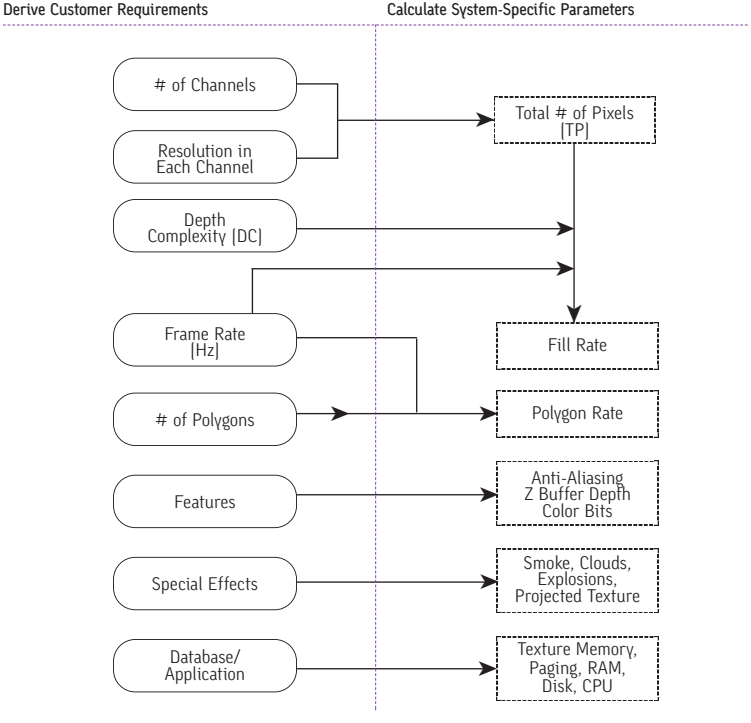
InfiniteReality3™

POCKET CONFIGURATOR

Begin by Scoping the Application



Having derived the system parameters from the customer requirements, use the data in this card to determine the system configuration for the specific application.

Establishing Key Criteria in Detail

Number of Pipelines and Channels

Determine the number of pipelines and channels required.

Note: The number of graphic pipelines depends on the chosen SGI™ Onyx® chassis.

Choose the Display Generator:

- DG5-2 supports up to two channels per pipeline (standard)
- DG5-8 supports up to eight channels per pipeline (optional)
- DPLEX enables pipeline multiplexing for distortion correction and interactive large-model visualization (optional)
- GVO converts the analog graphics output of the pipe into uncompressed NTSC/PAL in real time (optional)
- HD-GVO converts the analog graphics output into HDTV in real time (optional)

Note: Only one Display Generator can be used per pipeline. DPLEX, GVO, and HD-GVO support a maximum of two graphics channels per pipeline.

Display Parameters

Determine the resolution for each channel (number of lines x number of pixels per line). Calculate the total number of pixels in each channel and the sum total number of pixels for all channels in the system. Determine the vertical refresh rate for each channel—for example, 60 Hz noninterlaced, 30 Hz interlaced, 180 Hz field sequential, and so on.

Frame Rate

Determine frame rate requirements in Hz for the update of the visual scene—typically 30 Hz or 60 Hz.

Depth Complexity (DC)

For a typical scene and resolution, determine how many times, on average, pixels are overwritten to the display area.

Typical Average Depth Complexity Values for Z Buffer

Fixed Wing/Maritime	2–3
Rotocraft Flight/Ground Warfare	4–5
Driving/Railroad Simulation	3–4
Fixed Eyepoint Simulation	1–2

Note: The application can be designed to take advantage of the dynamic resolution capability. A lower depth complexity can be used to configure the system with the assumption that in pixel fill stress situations, the system will reduce resolution in the channel to maintain the frame rate.

Common Questions

Is anti-aliasing (aa) required? How many subsamples: four or eight?

How many bits per color component: RGB or RGBA? 10 or 12? 16-bit monochrome (I16) is also available.

What is the Z buffer resolution: 32-bits or compressed Z buffer?

Are there any special effects requirements that increase depth complexity and affect the configuration—for example, smoke, multiple cloud layers, 3D texture use, or projected texture use?

Are there special features that require large-capacity texture memory, extra disk, or CPUs, e.g., geospecific texturing, large-area database paging, or database intersections?

For more information consult the SGI Onyx Technical Report. For help with configurations with calligraphic lights, distortion correction, other special features, and RealityMonster® configurations, contact Visual Solutions Marketing.

Calculating the System Parameters

Allocating Channels and the Number and Type of Raster Managers (RMs) per Pipeline
Use the system design criteria and the rules below regarding fill rate, video bandwidth, frame buffer size, texture memory size, and polygon throughput to allocate channels and the number and type of RMs per graphics pipeline. TPP = total number of pixels per pipeline.

Fill Rate

TPP = (channel resolution) x (number of channels) + (channel resolution) x (number of channels) + …
Total fill rate = TPP x Hz x DC
Total fill rate/fill rate per RM = number of RMs

Fill rates for number of RMs (millions pixels/second), anti-aliased (aa), compressed Z buffer, fully visible textured pixels.

Type	1 RM	2 RMs	4 RMs
InfiniteReality3™ (8 subsample aa)	165–185	330–370	660–740

For typical applications with mixed texture map size, use low-average pixel fill rate for calculations.

Frame Buffer Memory (pixels and MB per RM)	256-Bit Small Pixels	512-Bit Medium Pixels	1024-Bit Large Pixels	Frame-Buffer Memory per RM
InfiniteReality3	2560K	1280K	640K	80MB

Adding RMs increases total frame-buffer memory.

Texture Memory

InfiniteReality3 RMs have 256MB of texture memory.
A useful map size can be as small as 16x16.

Sample Texture Size	Number of 16-Bit Mipmap Textures (256MB RM)
1024x1024	64
512x512	352
256x256	1504
128x128	6112

Adding RMs does not increase total texture memory capacity.

Video Bandwidth (BW)

Maximum frame buffer to display generator (DG) bandwidth:

- 290M pixels/sec for 10-bit RGB and 12-bit color field sequential
- 210M pixels/sec for 12-bit RGB and 10-bit RGBA
- Channels 0 and 1, DAC output BW = 220M pixels/sec per channel
- Channels 2–7, DAC output BW = 170M pixels/sec per channel

Adding RMs does not increase frame buffer to video subsystem bandwidth.

Format BW = total number of lines (including vertical blanking) x number of active pixels/line x frame rate. The total number of lines is part of the Video Output Format (VOF) specification.

E.g., for 640x480_60 (60 Hz noninterlaced):

Format BW = 525 lines x 640 pixels/line x 60 = 20.16 MHz

If necessary, add pixels to the number of active pixels/line to make the number divisible by 160—required for data transfer.

Format Combinations

The following format combinations are allowed within a pipeline if:

a) Sum of the BW does not exceed pipeline RM to DG or DG to DAC BW
b) Basic swap interval is an integral multiple—for example 60 Hz/30 Hz/20 Hz
c) Frame buffer size is not exceeded
d) Maximum number of channels per pipeline is not exceeded

Use the VOF combiner tool to validate combinations.

Polygon Rate

Polygon rate per pipeline = the sum of all polygons in each channel x frame rate (Hz).
The polygon rate per InfiniteReality3 pipeline is approximately 1035K to 1550K* (K=thousands) polygons per second.

Pipeline polygon throughput (number of aa, textured, potentially visible):

InfiniteReality3	35K–50K* @ 30 Hz	17K–30K* @ 60 Hz

Allocating CPUs

General rule: 2 CPUs per graphics pipeline

- 1—draw
- 1—cull/app or multiple culls

1 CPU for IRIX® and other nondeterministic processes
Additional CPUs for host functions and/or special features, such as database paging, intersections, and calligraphic lightpoints

Note: 1) SGI Onyx 3000 series systems require one C-brick per pipeline.

2) SGI Onyx 3400 and 3800 configurations require 4 CPUs per C-brick.

*While original benchmark numbers remain valid, these values are rated for achievable performance in an application environment.

Use the calculations and criteria above to check that the application will function for each pipeline; if necessary, transfer channels to additional pipelines or systems.