

Interphase
4511/5511 Adapter
Hardware Functional
Specification



4511/5511

PMC/PCI FDDI DIRECT CONNECT CARD

Hardware Functional Specification

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Authors: Craig Botkin Steve Kappes

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1.0 TERMINOLOGY

MIC	Media Interface Connector
STP	Shielded Twisted Pair
UTP	Unshielded Twisted Pair
PMD	Physical Layer Medium Dependent
PHY	Physical Layer Protocol
FCG	FDDI Clock Generator
ELM	Elasticity buffer and Link Management
MAC	Media Access Controller
FSI	FDDI System Interface
CMT	Connection Management
SMT	Station Management
PCI	A specification defined for Peripheral Component Interconnect. The document this product adheres to is listed in Section 4.1.
PMC	PMC is a physical variant of the PCI specification. The PMC version of this product (4511) is electrically and functionally identical to the PCI version of this product (5511). Any reference to either PCI or PMC shall be applicable to the other unless otherwise noted.

2.0 REFERENCES

2.1 Components

Motorola MC68836 FCG User's Manual printed November 1991

Motorola MC68837 ELM User's Manual printed December 1991

Motorola MC68340 User's Manual Rev 1 printed April 1992

Motorola MC68840 IFDDI User's Manual printed June 1993

3.0 ENVIRONMENT

3.1 Hardware Environment

Power:	5VDC +/- 5% @ x.x Amps maximum
	12VDC +/- 5% @ 0.034 Amps maximum
	-12VDC +/- 10% @ 0.034 Amps maximum

3.1.1 Miscellaneous

The product will operate with a PCI bus clock of any frequency within the limits specified in the PCI specification referred to in Section 4.1.

3.2 Physical Environment

3.2.1 Mechanical Specifications

The 4511 will conform to the PMC specification. The 5511 will conform to the PCI short card specification. The documents are listed in Section 4.1.

3.2.2 Environmental Specifications

Operating Temperature:	0 to 55 degrees C
Storage Temperature:	-40 to 125 degrees C
Operating Humidity:	10 to 90% non-condensing
Operating Altitude:	3,048 meters (10,000 feet) maximum
Storage Altitude:	15,240 meters (50,000 feet) maximum

3.3 Standards

PCI Local Bus Specification	Version 2.0	April 30,1993
CMC	Draft 2.0	April 4,1995
PMC	Draft 2.0	April 4, 1995
FDDI PHY Specification	ANSI X3.148-1988	June 30, 1988
FDDI SMF-PMD Specification	X3T9.5/88-155 Rev 4.2	May 18, 1990
FDDI MAC Specification	ANSI X3.139-1987	November 5, 1986
FDDI SMT Specification	X3T9.5/84-49 Rev 7.2	June 25, 1992

4.0 Byte Ordering

The PCI bus uses Little-endian byte ordering and the Motorola 68340 processor uses Big-endian byte ordering. The PCI bus host and the onboard processor communicate through common shared memory.

The byte lanes between shared memory and the PCI bus are not manipulated by hardware in any manner. The table describes the data bits addressed from the PCI bus.

TABLE 1. PCI Bus Little-Endian Byte Ordering

Data Bit 31 ----- 24	Data Bit 23 ----- 16	Data Bit 15 ----- 8	Data Bit 7 ----- 0	ADDRESS
xxxxxxx	xxxxxxx	xxxxxxx	xxxxxxx	Doubleword
		xxxxxxx	xxxxxxx	Word 0
xxxxxxx	xxxxxxx			Word 1
			xxxxxxx	Byte 0
		xxxxxxx		Byte 1
	xxxxxxx			Byte 2
xxxxxxx				Byte 3

The byte lanes between shared memory and the onboard processor are not manipulated by hardware in any manner. The table describes the data bits addressed from the onboard processor.

TABLE 2. Motorola Big-Endian Byte Ordering

Data Bit 31 ----- 24	Data Bit 23 ----- 16	Data Bit 15 ----- 8	Data Bit 7 ----- 0	ADDRESS
xxxxxxx	xxxxxxx	xxxxxxx	xxxxxxx	Longword
xxxxxxx	xxxxxxx			Word 0
		xxxxxxx	xxxxxxx	Word 1
xxxxxxx				Byte 0
	xxxxxxx			Byte 1
		xxxxxxx		Byte 2
			xxxxxxx	Byte 3

5.0 PERFORMANCE

5.1 Performance Requirements

5.1.1 PCI Bus

The PCIFIC will allow for zero wait state bursts at the full PCI bus burst rate. As a slave, the PCIFIC will generally provide for slave latencies of less than 16 clocks.

5.1.2 Onboard Processor

An onboard processor will offload SMT processing from the host processor. The onboard processor is not in the LLC data path. The onboard processor will perform SMT functions within SMT specified times. Refer to Section 6.7 for more detail.

5.1.3 LLC Traffic

LLC traffic is handled by the host processor directly controlling the FDDI front end chip set. LLC traffic is transferred to the PCI bus directly by the IFDDI.

The 4511/5511 executes from descriptor rings residing in host memory. It reads descriptor ring entries, executes commands and writes indications back to host memory. The host need not acquire the PCI bus to write descriptor ring entries or to read indications. The host does acquire the PCI bus to initiate descriptor ring execution and to acknowledge interrupts.

6.0 FUNCTIONALITY

6.1 Functional Capability

6.1.1 Requirements

The 4511/5511 FDDI controller will meet the following requirements:

- Single Attach Station (SAS)
- Inexpensive
- High performance
- 128KB local buffer
- SMT processor onboard

6.1.2 Options

The 4511/5511 FDDI controller will have the following options:

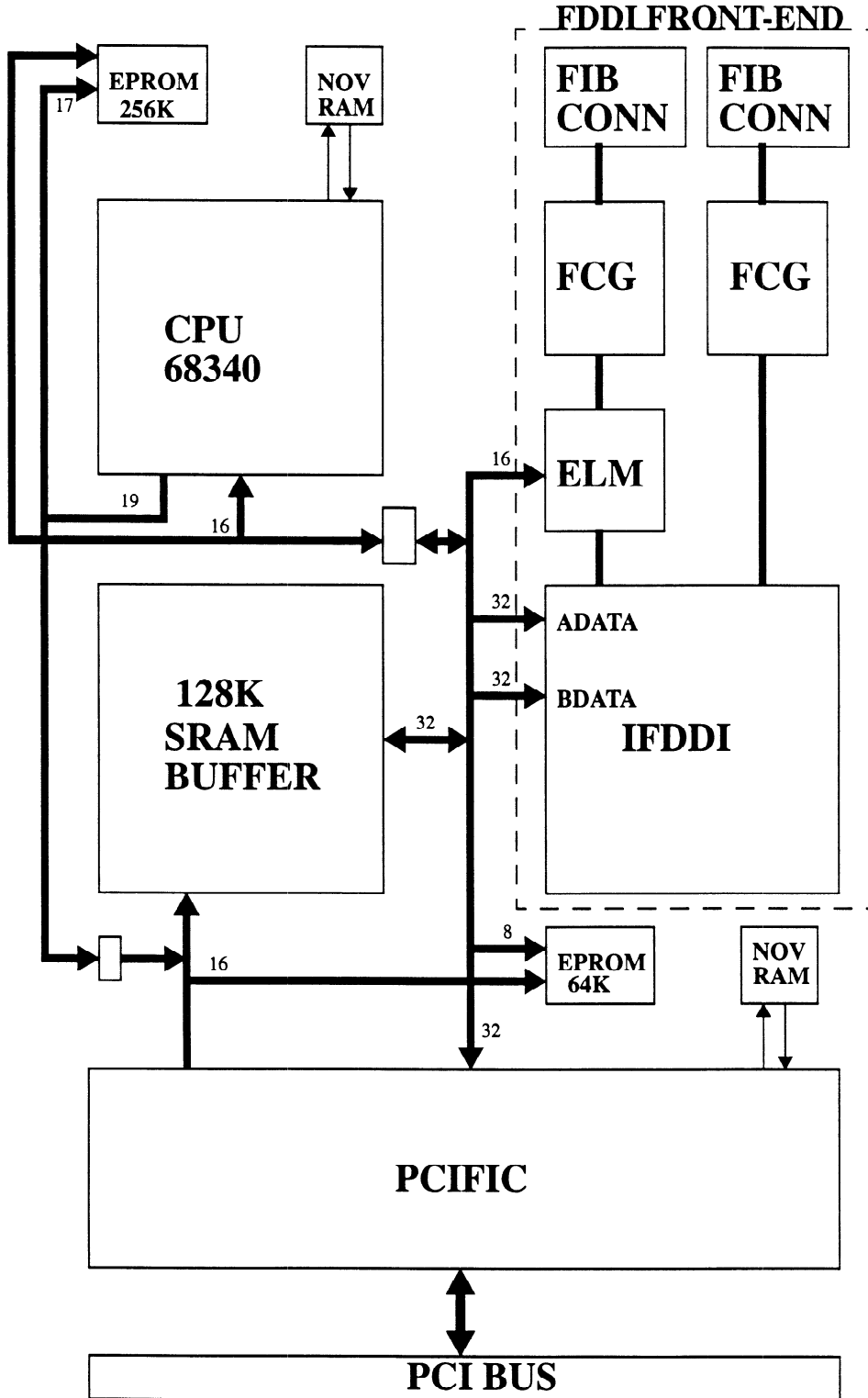
- MIC, STP or UTP media interface
- Flash memory for onboard processor

6.1.3 Features on the 5511 but not on the 4511

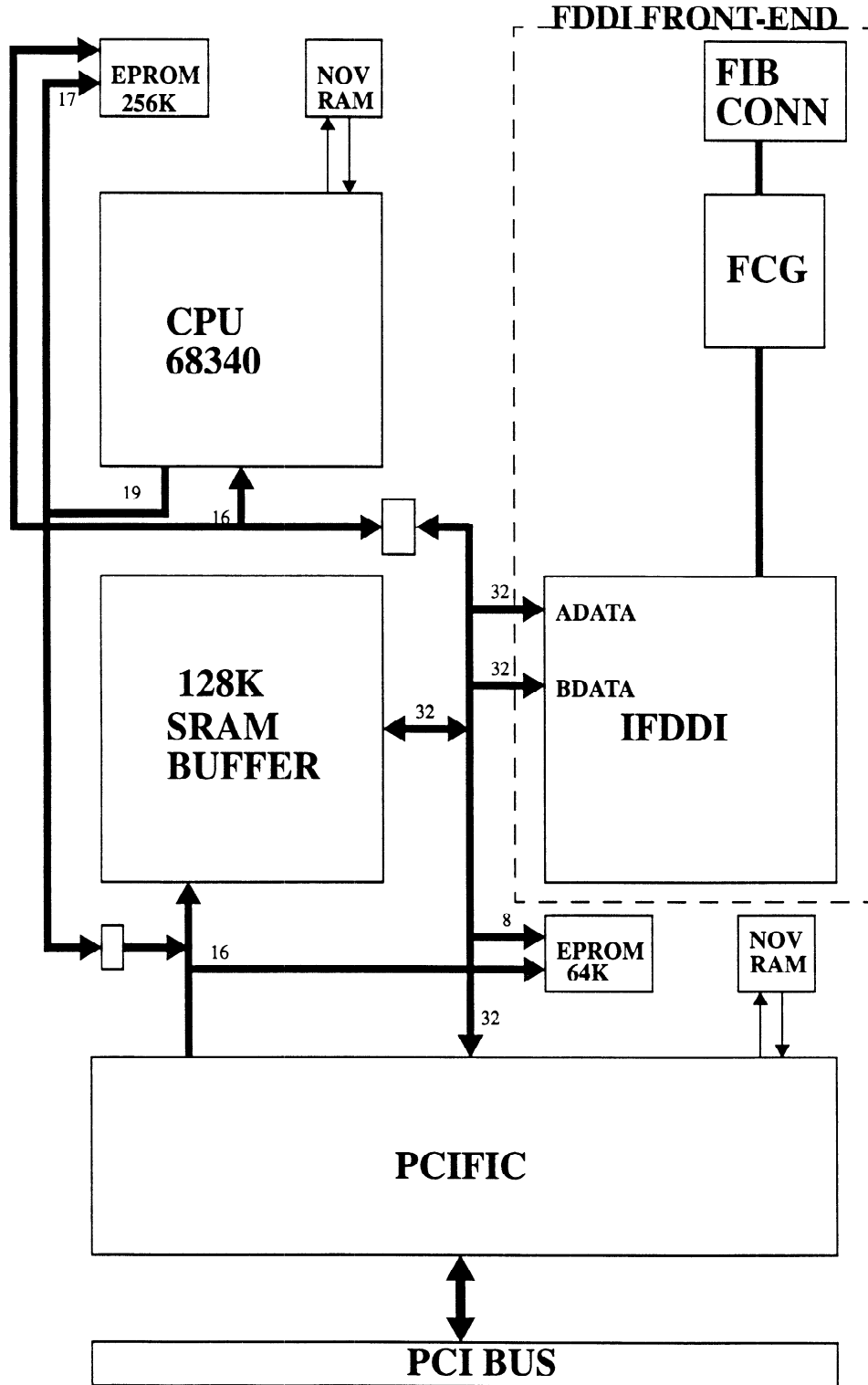
The following will be supported on the PCI FDDI, but not on the PMC FDDI:

- Dual Attach Station (DAS)
- Optical bypass control

6.2 BLOCK DIAGRAM (DAS) PCI 5511



6.3 BLOCK DIAGRAM (SAS) 4511/5511



6.4 FDDI Front End

The FDDI Front-End consists of the Motorola 68840 IFDDI and the Motorola 68836 clock generator. The 5511 may also use the Motorola 68837 ELM and a second 68836 to provide DAS support. The physical connection may be one of the following.

- MIC fiber connector
- STP (Shielded Twisted Pair) connection
- UTP (Unshielded Twisted Pair) connection

6.5 PCIFIC

6.5.1 PCI Features

The PCIFIC handles all PCI bus accesses. The PCIFIC interprets and generates all PCI signals in accordance with the PCI specification Rev. 2.0. The following PCI features are supported.

- PCI specification rev 2.0 compliant
- Meets PCI Compliance Checklist
- 32 bit 0 wait state Master for up to 132Mbyte/s burst DMA rate
- 32 bit Slave
- Supports Expansion Rom
- Configuration space and IEEE Address initialized from external serial EEPROM
- 128 Byte Receive FIFO and 64 Byte Transmit FIFO for DMA Master

6.5.2 PCI Master Bus Cycles Supported

The PCIFIC supports only the relevant PCI bus cycles. These cycles are defined by the $\overline{C}/\overline{BE}[3:0]$ command lines during the address phase of each PCI bus cycle. The following table shows these bus cycles and the mode supported by the PCIFIC. Note that bus cycles with an asterisk are ignored by the PCIFIC.

TABLE 3.

$\overline{C}/\overline{BE}[3:0]$	Bus Cycle Type	Mode Supported
0000	Interrupt Ack	*
0001	Special Cycle	*
0010	I/O Read	*
0011	I/O Write	*
0100	Reserved	*
0101	Reserved	*
0110	Memory Read	Master / Target
0111	Memory Write	Master / Target
1000	Reserved	*
1001	Reserved	*
1010	Configuration Read	Target
1011	Configuration Write	Target
1100	Mem Read Multiple	Master
1101	Dual Address Cycle	Master
1110	Memory Read Line	Master
1111	Memory Write and Invalidate	Master

6.5.3 PCI Slave features supported

As a slave, the PCIFIC will respond to Configuration, and Memory cycles. The PCIFIC does not respond to I/O Cycles. The PCIFIC does not do PCI slave bursting. If a burst is attempted to the PCIFIC, it will terminate the cycle after the first data transfer.

- The PCIFIC PCI BIU slave interface has the following features:
- Supports memory and configuration cycles
- Supports optional Expansion Rom
- Supports write posting
- Configuration and other registers loaded from external serial EEPROM
- Single access only, no bursting supported.
- Meets PCI worst case latency guidelines (16 clocks max)

6.5.4 PCI Master transfer data alignment restrictions

No odd byte or word alignment is performed beyond the capabilities of the Motorola FDDI chip set. Transmit buffers can start on any byte alignment. The FDDI system interface chip will transfer full 32-bit doublewords and use only the bytes which are valid as indicated by the buffer starting address and length. Receive buffers always begin on 32-bit doubleword boundaries. Receive buffers with odd byte or word lengths contain indeterminate data to buffer end. Any alignment required by the host or onboard processor must be performed by the host or onboard processor.

No byte manipulation is performed during shared memory transfers. Shared memory content will be the same for a doubleword, 2 word or 4 byte transfer. Little endian byte ordering is maintained between shared memory and the EISA bus. Byte lane 0 is data bits 7 through 0 and byte lane 3 is data bits 31 through 24.

The onboard SMT processor must complete initialization before the board becomes ready.

6.6 Local Buffer

The local buffer supports a single bank of 32Kx8 asynchronous RAMs. This provides for 128K bytes of local storage for use by the on board SMT processor. This buffer is also used for the shared memory required for the host processor to communicate with the onboard SMT processor.

6.7 SMT Processor

The SMT Processor runs SMT locally, offloading the host CPU. The following features are required.

- Motorola 68340 processor - 25MHz
- Two serial ports
- Two byte-wide EPROMs
- Optional Flash replaces EPROMs
- Nonvolatile configuration memory
- Background debug mode

The processor executes out of EPROM or Flash. It uses buffer memory for stack and variables. EPROM is removed when Flash is populated. Flash is segmented to allow portions to be erased while executing out of Flash for firmware updates.

The processor can not access the PCI bus.

Background debug mode enables the processor to be controlled through a special full duplex serial channel. Only a few pins need be operational to enable control of the processor for debug and possibly firmware download to Flash.