6224 VME
100Base-T Adapter
Users Guide

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	Fax:	(214) 654-5500
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	Fax:	44 (0) 1869-247720
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	Support:	(81) 3-5423-6514

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product, must observe all stated warnings and safety precautions in order to safely operate the equipment in your environment.

Do Not Substitute Parts or Modify Equipment

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Interphase representative for service and repair to ensure that safety features are maintained.

Ground the Instrument

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

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Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep away from Live Circuits

Do not install or replace the component with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Observe Dangerous Procedure Warnings

Warnings precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Declaration of Conformity

(according to ISO/IEC Guide 22 and EN 45014)

Manufacturer's Name:	Interphase Corporation
Manufacturer's Address:	13800 Senlac Dallas, Texas 75234 U.S.A.

declares, that the product:

Product Name: VME 100MB TX Ethernet

Model Number: 6224

conforms to the following Standards:

Safety:	EN 60950:1988 + A1, A2
EMC:	EN 55022:1988 class A EN 50082-1 Part 1 1992

Supplementary Information:

This product complies with the requirements of the **Low Voltage Directive 73/23/EEC** and the **EMC directive 89/336/EEC**.

Dallas, July 19, 1996

Mike Jobe, Quality Manager

European Contact:

Interphase International
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Preface

Inside This Users Guide

This users guide is organized as follows:

Chapter 1, *Introduction*, provides general information about the 6224 VME 100Base-T adapter, its features, and its system requirements.

Chapter 2, *Installing the 6224 Adapter*, explains how to install the adapter.

Chapter 3, *Cabling and Connectors*, explains how to attach the cables and connectors for the daughtercard(s).

Chapter 4, *Installing the 6224 HP-UX Driver*, explains how to install the driver.

Chapter 5, *Troubleshooting the 6224 Adapter*, provides possible solutions for when you are having problems installing or operating the adapter.

Appendix A, *6224 Specifications*, provides specifications for the adapter.

Appendix B, *VME Technology Overview*, contains an overview of VME technology, which relates to this adapter's motherboard.

Appendix C, *PCI/PMC Technology Overview*, contains an overview of PMC technology, which relates to this adapter's daughtercard(s).

Appendix D, *100Base-T Technology Overview*, contains an overview of 100Base-T technology, which relates to this adapter's daughtercard(s).

The **Glossary** defines common acronyms and terms related to this adapter's VME, PMC, and 100Base-T technologies.

Icon Conventions

Icons draw your attention to especially important information:

Note

The Note icon indicates important points of interest related to the current subject.

Caution

The Caution icon brings to your attention those items or steps that, if not properly followed, could cause problems in your machine's configuration or operating system.

Warning

The Warning icon alerts you to steps or procedures that could be hazardous to your health, cause permanent damage to the equipment, or impose unpredictable results on the surrounding environment.

Text Conventions

The following conventions are used in this manual. Computer-generated text is shown in typewriter font. Examples of computer-generated text are: program output (such as the screen display during the software installation procedure), commands, directory names, file names, variables, prompts, and sections of program code.

```
Computer-generated text example
```

Commands to be entered by the user are printed in **bold Courier** type. For example:

cd /usr/tmp

Pressing the return key (↵ **Return**) at the end of the command line entry is assumed, when not explicitly shown. For example:

/bin/su

is the same as:

/bin/su ↵ Return

Required user input, when mixed with program output, is printed in **bold Courier** type. References to UNIX programs and manual page entries follow the standard UNIX conventions.

When a user command, system prompt, or system response is too long to fit on a single line, it will be shown as

```
Do you want the new kernel moved into
\ vmunix?[y]
```

with a backslash at either the beginning of the continued line or at the end of the previous line.

Introduction 1

Overview

Your 6224 VME 100Base-T adapter allows you to create one or more high-speed connections between your VMEbus-based HP-UX® system and your 100Base-T network. The 6224 adapter supports a data rate of 100 Mbps. The 6224 adapter consists of a 6200 VME to PCI bus bridge motherboard and either one or two 4524 PMC 100Base-T daughtercards.

All of the 6200 motherboard's VMEbus features are fully programmable from the VMEbus side. The 6200 supports read-modify-write cycles on the VMEbus. With its other VMEbus functions, the 6200 provides full VME interrupt and multilevel requester capabilities.

The 4524 daughtercard adapter adheres to the PMC (PCI Mezzanine Card) mechanical layout for use in mezzanine systems such as the 6200 VME motherboard.

The 6224 provides full auto-negotiation capabilities, selecting full or half duplex for 100 Mb or 10 Mb connections, and supports TX (category 5 UTP copper cable) or T4 (4-pair category 3 UTP copper cable).

Product Features

Motherboard

- 6U or 9U compatibility. Because of its 6U form factor, this product can be installed in 6U and (with an adapter) 9U VMEbus card cages.

- 2 PMC population sites, for either 2 TX daughtercards or 2 T4 daughtercards, thus allowing for 2 independent network connections
- Fully compliant, 32-bit, 33 MHz PCI local bus interface
- Fully compliant 64-bit high performance VMEbus interface
- Integral FIFOs for write posting to maximize bandwidth utilization
- Programmable DMA controller with linked list support
- VMEbus transfer rates of 60-70 MBps
- Complete suite of VMEbus address and data transfer modes
  - A32/A24/A16 master and slave
  - D64 (MBLT)/D32/D16/D08 master and slave
  - BLT, ADOH, RMW, LOCK
- Flexible register set, programmable from the VMEbus port
- Implements all of the addressing and data transfer modes documented in the VME64 specifications (except A64 and those modes intended to support 3U applications—A40 and MD32)

Daughtercard(s)

- Single Compu-shield® connector with RJ-45 cable converter for PMC, combining both 100Base-T and 10Base-T UTP
- Conforms to IEEE 802.3u 100Base-T standards and IEEE 802.3u 10Base-T standards
- Fully PMC compliant

- Supports 100 Mbps over existing category 3 wiring (T4)
- Supports 100 Mbps over existing category 5 wiring (TX)
- Auto-selects 100 Mbps or 10 Mbps over a single physical port
- Adaptive FIFO buffering
- Four LEDs on each PMC daughtercard for status monitoring
- Multiprocessor support
- Multicast support
- Optional EEPROM interface enables easy implementation of jumperless product
- 1.5KB RX and TX FIFOs
- Full auto-negotiation capability
- Conforms to IEEE 802.3u 100Base-T standards
- Ethernet and Token Ring frame support
- Supports 100Base-T or 10Base-T
- Plug-and-play compatible

System Requirements

System requirements for the 6224 adapter are as follows:

- Approximately 200K of free disk space for driver installation
- VME-based system

Installing the 6224 Adapter

2

Overview

Installing the 6224 adapter involves 4 basic steps:

1. Inspect the board.
2. Set onboard jumpers.
3. Power off system.
4. Install the board.

Inspect the Board

Caution

Handle the 6224 adapter carefully; the card is sensitive to static electricity. Interphase ships the board in an anti-static bag. Do not touch the adapter's components or metal parts (hold the adapter by its edges). To prevent card damage from electrostatic discharge, wear a grounding strap.

Remove the 6224 from its anti-static bag, and visually inspect it to ensure that no damage has occurred during shipment. A visual inspection is usually sufficient, as Interphase thoroughly checks each board just prior to shipment.

If the board is undamaged, proceed with the installation. If the board is damaged, refer to the Assistance information at the front of this manual. In addition to contacting your reseller or Interphase, contact the carrier (for example, UPS or Federal Express) that delivered the package.

Warning

Do not install, or apply power to, a damaged board. Failure to observe this warning could result in extensive damage to the board and/or the system.

Set Onboard Jumpers

Set the onboard jumpers so that the 6224 is properly configured for operation in your system. Figure 2-1 on page 7 shows the location of the jumpers. In this manual, IN refers to the jumper being installed across the pins indicated; OUT indicates that the jumper is removed.

Note: The boxed pins are pin position #1

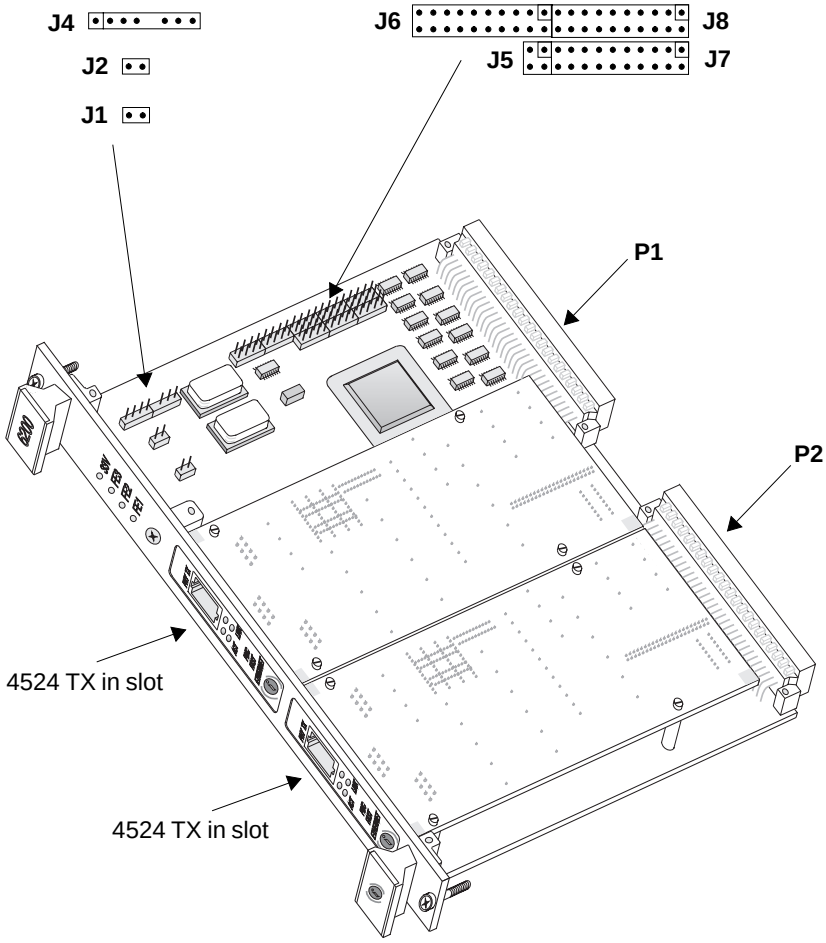

Figure 2-1. 6200 Motherboard Jumper Pins

Jumper Blocks for Interphase Use Only

The following jumper blocks are for Interphase use only:

- J1, Board Reset Switch (for debugging only)
- J2, PCI Bus Reset Switch (for debugging only)
- J4, In-System Programming Header

Reserved Jumper Blocks and Pins

The following jumper blocks are reserved:

- J5
- J6

J7 pins 3 and 4 through 19 and 20 are reserved.

Note

In jumper blocks J5 through J8, pin 2 is directly underneath pin 1 (see Figure 2-1 on page 7).

Jumper Blocks J7 and J8

Use these jumper blocks to

- Choose VME address space
- Set base address space for VME bus register slave image

Required

J8 pins 1 and 2 must be IN to enable the slave register image. This is the default.

VME Address Space

To choose VME address space:

To choose this VME address space . . .	J8 pins 3 and 4	J8 pins 5 and 6
A16	OUT	OUT
A24	OUT	IN
A32	IN	OUT

Base Address Space

Set the following jumpers to select the short I/O space the board will respond to, according to the VME address space you chose:

These pins . . .	Represent this bit if you chose A16 . . .	Represent this bit if you chose A24 . . .	Represent this bit if you chose A32 . . .
J8 pins 7 and 8	A15	A23	A31
J8 pins 9 and 10	A14	A22	A30
J8 pins 11 and 12	A13	A21	A29
J8 pins 13 and 14	A12	A20	A28
J8 pins 15 and 16	n/a	A19	A27
J8 pins 17 and 18	n/a	A18	A26
J8 pins 19 and 20	n/a	A17	A25
J7 pins 1 and 2	n/a	A16	A24

Note

If you choose A16, the system provides bits A11 through A8.

A16 Example

If you choose VME address space A16 and want the board to respond to the short I/O space 8000, you would set your block J7 and J8 jumpers as follows:

Pins	Setting
J8 pins 1 and 2	IN
J8 pins 3 and 4	OUT
J8 pins 5 and 6	OUT
J8 pins 7 and 8	IN
J8 pins 9 and 10	OUT
J8 pins 11 and 12	OUT
J8 pins 13 and 14	OUT
J8 pins 15 and 16	OUT
J8 pins 17 and 18	OUT
J8 pins 19 and 20	OUT
J7 pins 1 and 2	OUT
J7 pins 3 and 4 through 19 and 20	n/a (Reserved)

A24 Example

If you choose VME address space A24 and want the board to respond to the short I/O space 800000, you would set your block J7 and J8 jumpers as follows:

Pins	Setting
J8 pins 1 and 2	IN
J8 pins 3 and 4	OUT
J8 pins 5 and 6	IN
J8 pins 7 and 8	IN
J8 pins 9 and 10	OUT
J8 pins 11 and 12	OUT
J8 pins 13 and 14	OUT
J8 pins 15 and 16	OUT
J8 pins 17 and 18	OUT
J8 pins 19 and 20	OUT
J7 pins 1 and 2	OUT
J7 pins 3 and 4 through 19 and 20	n/a (Reserved)

A32 Example

If you choose VME address space A32 and want the board to respond to the short I/O space 80000000, you would set your block J7 and J8 jumpers as follows:

Pins	Setting
J8 pins 1 and 2	IN
J8 pins 3 and 4	IN
J8 pins 5 and 6	OUT
J8 pins 7 and 8	IN
J8 pins 9 and 10	OUT
J8 pins 11 and 12	OUT
J8 pins 13 and 14	OUT
J8 pins 15 and 16	OUT
J8 pins 17 and 18	OUT
J8 pins 19 and 20	OUT
J7 pins 1 and 2	OUT
J7 pins 3 and 4 through 19 and 20	n/a (Reserved)

Power Off System

Once the board is configured, ensure that the host system and peripherals are turned off.

Caution

System power and peripheral power must be turned off before attempting to install the 6224. Failure to do so can result in severe damage to the board and/or the system.

Install the Board

Install the 6224 adapter as follows:

1. Carefully slide the 6224 into the VMEbus card slot. It should slide all the way in without any difficulty.
2. Once the board is properly seated in the slot, tighten the captive mounting screws on each end of the front panel.

Cabling and Connectors 3

Cables for 100Base-TX and 100Base-T4

Incorrectly wired or installed cabling is the most common cause of communications problems for local area networks. Interphase recommends that you work with a qualified cable installer for assistance with your cabling requirements.

For each daughtercard, connect the appropriate cable to the 4524 daughtercard and to the hub.

Use unshielded twisted-pair cables that comply with the IEEE 802.3 100-Mbps standard. This standard supports cabling up to 100 meters only.

Caution

The cables used with the 6224 adapter must comply with 802.3u standards in order to meet emissions requirements.

100Base-TX UTP requires 2-pair Category 5 cabling. 100Base-T4 UTP requires 4-pair Category 3 (or better) cabling.

Compu-shield Connector Pinouts

This section includes pin-out information for twisted-pair connectors. Connectors on LAN adapters adhere to appropriate standards agreed upon by various standards bodies, and are widely available. The PMC specification does

not allow for the standard RJ-45 jack for network connections, so the 4524 adapter uses a Compu-shield connector to provide connectivity. An external cable is available for converting to an RJ-45 physical form factor.

Table 3-1. 100Base-TX Pinouts

Pin	Signal	Description
1	TX+	Transmit
2	TX-	Transmit
3	RX+	Receive
4	n/a	Not Used
5	n/a	Not Used
6	RX-	Receive
7	n/a	Not Used
8	n/a	Not Used

Table 3-2. 100Base-T4 Pinouts

Pin	Signal	Description
1	TX_D1+	Transmit
2	TX_D1-	Transmit
3	RX_D2+	Receive
4	BI_D3+	Bidirectional

Table 3-2. 100Base-T4 Pinouts (continued)

Pin	Signal	Description
5	BI_D3-	Bidirectional
6	RX_D2-	Receive
7	BI_D4+	Bidirectional
8	BI_D4-	Bidirectional

Installing the 6224 HP-UX Driver

4

Overview

This chapter explains how to install the 6224 HP-UX driver and configure the 100Base-T network interface. This driver supports a maximum of one 6224 adapter (with either one or two 4524 daughtercards).

Installation Prerequisites

Before installing the 6224 adapter in your system, the following software, hardware, and network prerequisites must be met:

- **Software:**
  - HP-UX 10.10 or later
    You can verify the operating system by entering **`uname -a`**
  - You must be logged in as **`root`**
  - Approximately 1 megabyte of free disk space in the `/usr` directory
- **Hardware:**
  - Hewlett-Packard VME system
- **Installation device:**
  - Device name of the DDS tape drive

    The installation procedure assumes that the tape device `/dev/rmt/0m` is installed and is being used. If you are using another device, substitute the appropriate name.

- **Network:**
  - New IP address, subnet mask (optional), and host name alias for the 6224
  - Appropriate cables to connect the 6224 to the network
  - 100Base-T hub

Installing the Driver

Note

Depending on your terminal type, the keystrokes for navigating through the installation screens may vary. For more information, see your Hewlett-Packard documentation.

To install the driver using the `swinstall` program, do the following:

1. Ensure that there is a valid `vme.CFG` file in the `/sbin/lib/vme` directory. For detailed information on how to configure the `vme.CFG` file for your system, see your HP-UX system administrators guide.
2. Insert the software media (DDS tape) in the appropriate drive.
3. At the prompt, enter **`/usr/sbin/swinstall`**

   If the *Source Depot Path,* which typically defaults to `/dev/rmt/0m,` is not the device node for your tape drive, change the *Source Depot Path* to point to your tape drive.
4. Select **`OK`**.

The following message might appear:

```
The software view is set to show bundles, but no
bundles were found on the source "bay:/dev/rmt/0m".
The software will be shown as products.
```

This is normal; select **OK** if this message appears.

5. Highlight the **Interphase_6224** fileset (the only one available) and mark it for installation.

6. From the **Action** menu, select **Install (analysis)...**

7. Select **OK** when the analysis completes.

   `swinstall` prompts you with:

```
Installation will now begin ...

Do you wish to begin Installation?

[Yes]
```

8. Select **Yes.**

   `swinstall` displays the `Confirmation` dialog:

```
Before starting installation, you should be aware of
the following: Kernel filesets will be installed on
the local system. The installation process will
include building a new kernel.

Do you still wish to start Installation?

[Yes]
```

9. Select **Yes.**

When the installation is complete, `swinstall` builds a new kernel. The time needed to rebuild the kernel varies with each system. `swinstall` does not reboot your machine.

The `swinstall` portion of the installation is complete.

10. To update the VME EEPROM with 6224 driver information, enter **`vme_config`** at the command line.

Note

If you get a message similar to

```
Internal Error 200: VME device special file
"/dev/vme2_config" open failed
errno: 19, No such device
```

reboot the system, and run vme_config again.

11. Reboot the system.

12. Check the log file `/var/adm/sw/swagent.log` to see if there were any software configuration problems. Read any error messages and follow their instructions.

The software installation is complete; continue with the next section.

Configuring the Network Interface

Before the 6224 can communicate with other hosts on the network, its interface must be configured. The following procedure uses the HP `System Administration Manager` (SAM) program to configure the interface.

To invoke SAM at the HP-UX prompt, enter **`sam`**

SAM modifies your `/etc/rc.config.d/netconf` file with the interface IP address and netmask you supply. For information about configuring the network interface with SAM, see your Hewlett-Packard *Installing and Administering LAN/9000* manual.

After you configure the 100Base-T interface with SAM, the system will recognize the 6224 100Base-T interface.

The driver and adapter automatically sense the hub type and establish a connection (to a 10Base-T or 100Base-T hub).

Now that SAM has modified the `netconf` file, the 6224 driver will be automatically configured each time the system boots.

Verifying the Interface

If you used SAM, the interface verification takes place at bootup. However, if you chose to add the interface IP address and netmask information manually, you can use the `ifconfig` command to verify that the 6224 interface is up. If the 6224 is unable to communicate with other systems, see *Problems and Solutions* on page 29.

1. Use the `ifconfig` command to verify that the interface IP address and netmask are correct. For example: **`ifconfig ife4`**

```
ife4: flags=63<UP,BROADCAST,NOTRAILERS,RUNNING>
    inet 17.15.21.131 netmask ffffff00 broadcast 17.15.21.255
```

Figure 4-1. `ifconfig` Output Sample

2. To verify that the 6224 can communicate with other hosts, use the `ping (1M)` command. For example: **`ping 17.15.21.130`**

```
64 bytes from 17.15.21.130: icmp_seq=1. time=3 ms
64 bytes from 17.15.21.130: icmp_seq=2. time=1 ms
64 bytes from 17.15.21.130: icmp_seq=3. time=1 ms
:
:
```

Figure 4-2. `ping` Output Sample

Removing the Driver

Note

For more information about SAM and swremove, see your Hewlett-Packard documentation.

To remove the 6224 HP-UX driver from your system, do the following:

1. Use SAM to remove the driver from the system configuration.
2. To deinstall the software, enter **`swremove`**

Troubleshooting the 6224 Adapter

5

Overview

This chapter explains the daughtercard(s)' LEDs, describes some common problems, and offers possible solutions to these problems. If you are unable to resolve a problem you are experiencing, contact your network supplier.

Faceplates

The 6224 adapter's 4524 daughtercard comes in two versions:

- TX, for 100Base-TX
- T4, for 100Base-T4

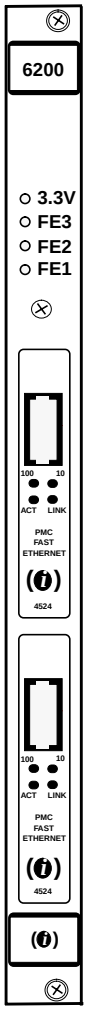

Figure 5-1. 6224 Adapter (with two 4524 TX) Faceplate

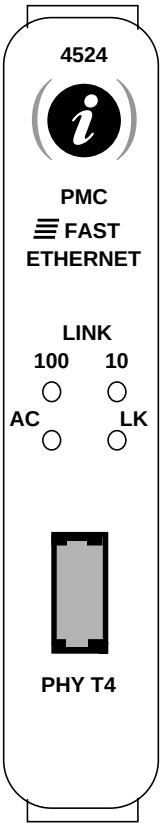

Figure 5-2. 4524 T4 Daughtercard Faceplate

LEDs

When this 4524 LED . . .	Is . . .	It means . . .
100	Off	100 Mb mode is off
100	Green	100 Mb mode is on
10	Off	10 Mb mode is off
10	Green	10 Mb mode is on
ACT	Off	No data is being transmitted or received across the cable.
ACT	Yellow	Data is being transmitted or received across the cable.
LINK	Off	There is no external link to the hub or the switch.
LINK	Green	There is an external 100 Mb or 10 Mb link made to the hub or the switch.

Problems and Solutions

Table 5-1. Troubleshooting

Problem	Possible solution(s)
The system does not recognize the adapter and no LEDs light	Check to ensure that the adapter is properly seated in the system backplane.
The LEDs light correctly, but the system does not recognize the adapter	**1.** Cycle power. **2.** Check configuration.
The system recognizes the adapter and its LEDs light correctly, but the adapter can't communicate with other systems	**1.** Verify that the cable being used complies with the IEEE 802.3u standard. **2.** Ping the broadcast address for the adapter interface and check to see if the activity light on the hub blinks. Other active hosts must be connected to the hub or the activity light does not blink.

6224 Specifications

A

Architecture

PCI-VME Bridge	Tundra® Semiconductor's Universe™
Local Buffer	512 KBytes

VMEBus Specifications

Capable data transfers	D32 BLT 30 MBps D64 MBLT 60 MBps
Address and data transfer modes	A32/A24/A16 D64/D32/D16/D08 BLT (Block Transfer) ADOH (Address-Only-With-Handshake) RMW (Read-Modify-Write) LOCK
Short I/O address	Jumper selectable

PCI Local Bus Specifications

- 33 MHz, 32-bit PCI local bus interface
- 2 sets of PMC connectors
- 5V only

Mechanical (Nominal)

The 6224 occupies one 6U single-height VMEbus slot.

Width	9.20" (233 mm)
Height	6.30" (160 mm)
Thickness	20 mm
Weight	357 g (2 daughtercards) 284 g (1 daughtercard)

Power Requirements

6224 with one daughtercard	2.0A at +5VDC
6224 with two daughtercards	2.9A at +5VDC

Operating Environment

Temperature	0–55° C / 32–131° F
Relative humidity	10–95% noncondensing
Altitude	-1000–15,000 feet
Air flow	250 LFM minimum

Storage Environment

This section assumes the adapter is stored in its original anti-static bag and box.

Temperature	-40–85° C / -42–185° F
Relative humidity	10–95% noncondensing

Altitude	-1000 to 50,000 feet

Cables and Connectors

Cable type	Connector type
Category 3 UTP (T4)	Compu-shield
Category 4 UTP (T4)	Compu-shield
Category 5 UTP (T4 or TX)	Compu-shield

Standards Compliance

IEEE	IEEE 802.3 Ethernet®

VME Technology Overview

B

VME Technology

VMEbus features a 32-bit address bus (up to 4 gigabytes of memory) and a 32-bit data bus, both of which can be dynamically configured. VMEbus also performs multiprocessing and can smoothly handle seven interrupt levels. VMEbus handles data transfers at speeds in excess of 40 MBps.

VMEbus uses a master-slave architecture. Masters transfer data to and from modules called slaves. Before a master can transfer data it must first acquire the bus using a central arbiter. This arbiter is part of the system controller. Its function is to determine which master accesses the bus next.

All bus activity is performed by the following four sub-busses:

- Data Transfer Bus
- Data Transfer Arbitration Bus
- Priority Interrupt Bus (interrupt processing)
- Utility Bus (16 Mhz clock and power-up reset)

For more information about VME terminology, see the glossary.

Obtaining VME Specifications

- VME64 Specification, available from:

  VME International Trade Association
  10229 North Scottsdale Road, Suite B
  Scottsdale, AZ 85253

- VMEbus Specification Revision D, IEEE, available from:

  IEEE Service Center
  Publications Sales Department
  445 Hoes Lane
  Piscataway, NJ 08854-4150

PCI/PMC Technology Overview

C

PCI/PMC Technology

A PCI bridge provides a high bandwidth path allowing PCI masters direct access to main memory. Intel® Corporation and the PCI SIG designed the PCI bus as the next generation I/O expansion bus. Its predecessors were ISA, EISA, and MCA. The PCI bus is a high-performance bus found in systems ranging from low-end PCs to high-end servers.

Three sizes of PCI add-in boards are defined: long, short, and variable short length. Systems are not required to support all board types. To accommodate the 5V and 3.3V signaling environments and to facilitate a smooth migration path between the voltages, three add-in board electrical types are specified: a “5 volt” board which plugs into only 5V connectors, a “universal” board which plugs into both 5V and 3.3V connectors, and a “3.3 volt” board which plugs into only 3.3V connectors.

The PMC bus was designed for embedded environments. It implements PCI bus logic in a daughtercard (mezzanine) form factor.

100Base-T Technology Overview

D

Overview

100Base-T is the IEEE 802.3u standard providing a 100-megabits-per-second data rate.

100Base-T technology is based on the CSMA/CD signaling used for 10Base-T. This standard allows auto- negotiation of speed and duplex configurations.

100Base-TX

The 100Base-TX adapter is based on specifications in the ANSI TP-PMD standard. 100Base-TX operates at 100Mbps over two pairs of wires. One pair is for receiving data; the other is for transmitting. The wire has an approximate impedance of 100 Ω. The wire is less than or equal to 100 meters in length.

The physical connection device (PHY) continuously monitors the receive data path for activity as a means of checking that the link is working correctly. This is done continuously during moderate to heavy traffic or even idle conditions on the network.

100Base-T4

The 100Base-T4 system operates over four pairs of wires. One pair is for transmitting data, one pair is for receiving data, and the remaining two pairs are bidirectional. So, for example, when data is being transmitted, the two bidirectional pairs and the transmit pair are all used for transmitting, while the receive

pair is used for sensing collisions. This makes it possible to provide Fast Ethernet signals over standard voice-grade Category 3 unshielded twisted-pair cable.

The 100Base-T4 media specification is designed to allow segments of up to 100 meters in length when using EIA/TIA Category 3, 4, or 5 unshielded twisted-pair cable. Category 5 cable allows fewer collisions due to its improved signal integrity.

The physical connection device (PHY) continuously monitors the receive data path for activity as a means of checking that the link is working correctly. When the network is idle, 100Base-T4 transceivers send link pulses over the segment to verify link integrity. These pulses are called Fast Link Pulses, and they are also used in the auto-negotiation mechanism,

which allows a multi-speed hub to detect the operation speed of an Ethernet device that is connected to it, and to adjust the speed of the hub ports accordingly.

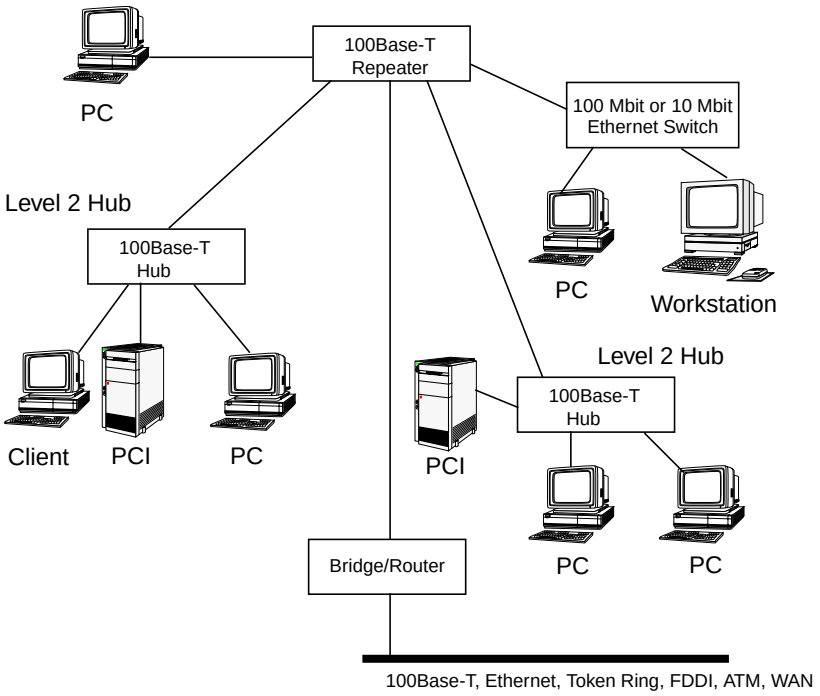

Figure D-1. Typical 100Base-T Network

Auto-Negotiation

Auto-negotiation is like a rotary switch that automatically switches to the correct technology (for example, 10Base-T or 100Base-TX Full Duplex). Once the highest-performance common mode is determined, auto-negotiation passes control of the cable to the appropriate technology and becomes

transparent until the connection is broken. Auto-negotiation leverages the proven link function of 10Base-T to provide robust operation over Category 3, 4, or 5 UTP.

The following lists define the priority hierarchy for resolving multiple common abilities. That is, if both devices support both 10Base-T and 100Base-TX, auto-negotiation at both ends will connect 100Base-TX instead of 10Base-T.

The priority hierarchy for TX mode is:

1. 100Base-TX Full Duplex
2. 100Base-TX
3. 10Base-T Full Duplex
4. 10Base-T

The priority hierarchy for T4 mode is:

1. 100Base-T4
2. 10Base-T Full Duplex
3. 10Base-T

To account for technologies that existed prior to auto-negotiation, auto-negotiation passes the signals present on the receiver to the 100Base-TX and 100Base-T4 Link Monitor functions.

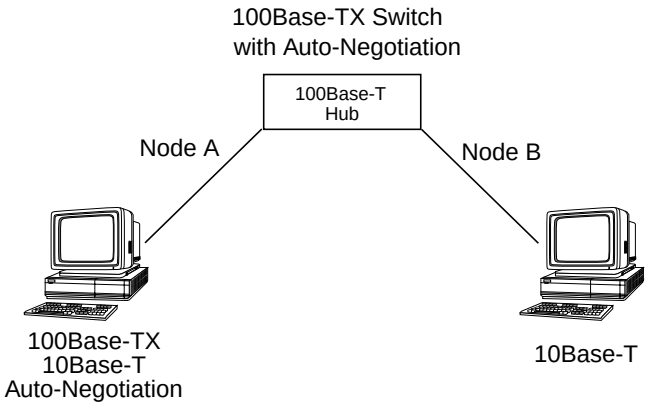

Figure D-2. Auto-Negotiation Basic Operation

World-Wide Web Resources

You can find information related to 100Base-T technology at the following web sites:

- `http://www.iol.unh.edu/consortiums/fe/fast_ethernet_consortium.html`
- `http://wwwhost.ots.utexas.edu/ethernet/100mbps.html`

Glossary

10Base-T

An IEEE 802.3 network specification using unshielded twisted pair cabling and running at 10 Mbps. 10Base-T recommends a maximum segment length of 100 meters.

100Base-T

A recent Fast-Ethernet technology developed by the IEEE 802-3 committee to increase the speed of standard networking from the existing 10Base-T Ethernet speeds. 100Base-T comes in two primary versions, TX and T4, as well as a fiber version.

100Base-TX

A version of 100Base-T technology that allows the use of only 2 pairs of wire, but because of the resulting signaling rates, it is limited to category 5 or better cabling installations. One pair is used for transmitting data and the other is used for receiving data or detecting collisions. The clock rate on each pair is 100 Mbits. The 100Base-TX version of the technology allows full-duplex implementations because of this balanced cable usage.

100Base-T4

A version of 100Base-T technology that uses 4 pairs of wire. By spreading the data across these pairs, it can be used over category 3 (or better) cabling. One pair is for transmitting data, one pair is for receiving data, and the remaining two pairs are bidirectional. So when data is being transmitted, the two bidirectional pairs and the transmit pair are all used for transmitting, while the receive pair is used for sensing

collisions. When data is being received, the two bidirectional pairs and the receive pair are all used for receiving. Note that since T4's use of the cable is asymmetrical, it cannot support Full Duplex configurations. Spreading the data across three pairs of wire allows each pair to operate at 33 Mbits and makes T4 more robust than TX in terms of noise immunity, signal loss, and cable quality.

5B/6B

The process of encoding (mapping) 5-bit data quintets into predetermined 6-bit symbols. This process is used to balance the data pattern to contain equal numbers of 0's and 1's, thus providing guaranteed clock transition synchronization for receiver circuitry.

5B/6B encoding provides added error-checking capability, which allows detection of invalid symbols, such as symbols with more than three 1's or 0's in a row.

A16

A module that uses address lines A01 through A15.

A24

A module that uses address lines A01 through A23.

A32

A module that uses address lines A01 through A31.

ACFAIL (AC Failure)

Indicates AC input to the power supply is no longer being provided.

AM0-AM5 (Address Modifier bits 0-5)

Used to broadcast address size, cycle type, and master identification.

Arbitration Bus

Coordinates use of the DTB.

ARP (Address Resolution Protocol)

The Internet protocol used to dynamically translate the Internet address of a network host to its LAN hardware address. This action is limited to LANs that support hardware broadcasts.

AS (Address Strobe)

Indicates a valid address on the address bus.

Attenuation

Signal power lost in a transmission medium as the signal travels from sender to receiver.

Auto-Negotiation

Auto-negotiation is a mechanism that takes control of the cable when a connection is established to a network device. Auto-negotiation detects the various modes that exist in the device on the other end of the wire (the Link Partner) and advertises its own abilities to automatically configure the highest performance mode of interoperation. As a standard technology, this allows simple, automatic connection of devices from a variety of manufacturers that support a variety of modes.

Backbone

A network configuration that connects LANs in order to form an integrated network.

Bandwidth

Bandwidth typically indicates a circuit's capacity for transmitting data. Generally, the greater the bandwidth, the more information can be sent through a circuit during a given amount of time.

BBSY (BUS Busy)

Driven true by the current master to indicate it is using the bus.

BCLR (BUS Clear)

Requests that the current master release the DTB.

BERR (BUS Error)

Indicates to the current master that the data transfer was not completed.

BG0IN-BG3IN (BUS Grant 0-3 In)

"Bus grant in" and "bus grant out" signals form bus grant daisy chains. The "bus grant in" signal indicates, to the board receiving it, that it can use the DTB.

BG0OUT-BG3OUT (BUS Grant 0-3 Out)

Indicates to the next board in the daisy-chain that it can use the DTB.

Bit

Binary Digit. The smallest unit of data that a computer can manipulate. A bit has two states, ON (1) and OFF (0).

block read cycle

Used to transfer a block of 1 to 1024 bytes from a slave to a master (256 transfers in 8, 16, or 32 bit width). The master broadcasts only one address and address modifier at the beginning of the cycle. The slave then increments this address on each transfer.

block write cycle

A DTB cycle used to transfer a block of 1 to 1024 bytes from a master to a slave (256 transfers in 8, 16, or 32 bit width). The master broadcasts only one address and address modifier at the beginning of the cycle. The slave then increments this address on each transfer.

BR0-BR3 (BUS Request 0-3)

Indicates that a master needs to use the DTB.

Bridge

An internetworking device used to connect two or more computer networks, and to forward packets among the networks.

Buffer

Temporary memory storage area set aside to hold frequently accessed data, or data to be processed.

Byte

An 8-bit unit of data. A byte is the smallest addressable unit of memory.

Client

A computer that uses resources provided by another computer, known as the server, on the network.

CRC (Cyclic Redundancy Check)

An error-checking procedure in which bytes at the end of a frame are used by the receiving node to detect transmission problems.

CSMA/CD (Carrier Sense Multiple Access/Collision Detect)

The low-level Ethernet network arbitration protocol. Ethernet nodes with data to transmit sense the link for a carrier signal. If such a node does not detect a carrier signal (that is, if the link is idle), the node begins transmitting its data on the link. While transmitting, the node listens. When two nodes transmit at once, the data gets corrupted. The nodes detect this and continue to transmit for a certain length of time to ensure that all nodes detect the collision. The transmitting nodes then wait for a random time before attempting to transmit again, thus minimizing the chance of another collision. The ability to detect collision during transmission reduces the amount of bandwidth wasted on collisions in comparison with simple broadcasting.

D00-D31 (Data Bus)

Bidirectional data lines used to transfer data between masters and slaves.

data transfer

Devices transfer data over the Data Transfer Bus (DTB).

Device Driver

The software program which enables a host computer to communicate with peripheral devices such as disk drives, network interface cards (NICs), and so on.

DMA (Direct Memory Access)

A fast method of moving data between the memory of two processor subsystems without processor intervention. The data transfer is done under hardware control.

DS0, DS1 (Data Strobe 0, 1)

Used in conjunction with LWORD and A01 to indicate how many data bytes are being transferred (1, 2, 3, or 4).

DTACK (Data Transfer Acknowledge)

Signal generated by a slave. Indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.

DTB (Data Transfer Bus)

The Data Transfer Bus allows masters to direct the transfer of data between themselves and slaves.

DTB arbitration

The Arbitration Bus modules (requesters and arbiter) that coordinate and control data transfer.

Fast Ethernet Consortium

The Fast Ethernet Consortium, hosted by the University of New Hampshire, tests Fast Ethernet (IEEE 802.3u) products and software from both interoperability and conformance

perspectives. For more information about the Consortium, see `http://www.iol.unh.edu/consortiums/fe/fast_ethernet_consortium.html`

Fast Link Pulses

Communication mechanism used in 10Base-T and 100Base-T networks to indicate link status and (in auto-negotiation equipped devices) to communicate information about abilities and to negotiate communication methods. 10Base-T uses Normal Link Pulses (NLPs), which indicate link status only. 10Base-T and 100Base-T devices equipped with auto-negotiation exchange information using a Fast Link Pulse mechanism which is compatible with 10Base-T.

Frame

A group of data bits in a specific format with flags at the beginning and at the end. It is a series of bytes sent with a header at the data link layer. Packets, on the other hand, refer to data at the network layer of the OSI stack and are considered to be contained inside a frame.

Full Duplex

A method of communication between two endpoints where data is transmitted simutaneously in both directions.

Gateway

Device used to connect two or more networks. The gateway routes the information among the networks.

Half Duplex

A method of communication between two endpoints where data is transmitted in only one direction at any given time.

Host

In general, any computer on a network. Host adapters are typically installed to provide a physical interface to the network. The host uses software to communicate with the adapter and to request the services of the adapter to transfer information to and from attached devices.

Host Adapter

A hardware device that provides the connection from the host computer bus to attached devices.

Hostname

A unique name that identifies each host machine on a network.

IACK (Interrupt Acknowledge)

Used by an interrupt handler acknowledging an interrupt request.

interrupt acknowledge cycle

Initiated by an interrupt handler that reads status/ID information from an interrupter.

IP (Internet Protocol)

A network layer protocol that contains addressing and control information to allow packets to be routed over dissimilar networks.

IRQ1-IRQ7 (Interrupt Request 1-7)

Generated by an interrupter.

KB (Kilobyte)

One KB or KByte is equivalent to 1024 bytes.

LLC (Logical Link Control)

The upper of the two sublayers of the OSI Reference Model's Data Link Layer. Defines the transmission of data between two stations with no intermediate switching nodes.

MAC (Media Access Control)

The part of the ISO model that describes how devices share access to a network. Ethernet, Token Ring, and FDDI are MAC-layer specifications. Wiring hubs deal primarily with MAC-layer equipment.

Master

Initiates DTB cycles.

MB (Megabyte)

One MB or Mbyte is equivalent to 1,048,576 bytes.

Mbps

Megabits per second (1,048,576 bits per second).

module

A functional board (master or slave) on the VMEbus.

Multicast

A technique that allows copies of a single packet or cell to be passed to a selected subset of all possible destinations.

Network

An interconnection of multiple stations or systems that are able to send messages to, or receive messages from, one another.

Network Interface

A defined path through a stack of protocols. In terms of hardware it is the device through which data packets are sent and received.

A network interface is identified by a name and a unit. The name and unit combine to form the interface identifier. The unit number can range from 0 to 4 (for example, lan0) due to a maximum of five LAN cards supported per system.

NIC (Network Interface Card)

An adapter that connects a station to a network.

NMS (Network Management Station)

The system responsible for managing a network or a portion of a network. The NMS communicates to network management agents residing in the managed node using a network management protocol.

Node

A device, such as a computer, station, or concentrator, that is connected to a network.

Packet

A group of bits, including data and control elements, that are transmitted together. Data is digitized (encoded) and transferred over LANs. Unlike voice and video

transmissions that require a minimum constant rate bandwidth, burst data can be transmitted in almost any order and reconstructed by the receiving node.

PCI (Peripheral Component Interconnect)

An Intel standard governing the connections and timings for a local bus that is 32 bits wide operating at 33 MHz. It brings high speed peripheral functions closer to the microprocessor while maintaining compatibility with traditional 16-bit expansion systems operating at 8 MHz.

PDU (Protocol Data Unit)

A sequence of contiguous bits delivered as a unit from the physical medium attachment sublayer. A valid PDU is at least 24 bits in length, and contains address fields and a control field.

Physical Layer

Layer 1 of the OSI reference model. Defines and handles the electrical and physical connections between systems. The Physical Layer can also encode data in a form that is compatible with the medium (coaxial, twisted pair, fiber, and so on).

PING (Packet Internet Groper)

A TCP/IP protocol facility used to test the reachability of destinations by sending an ICMP (Internet Control Message Protocol) echo request and waiting for a reply.

PMC (PCI Mezzanine Card)

A daughtercard form factor implementation of the PCI bus specification.

priority interrupt

Interrupt requests can be assigned one of seven priority values.

Priority Interrupt Bus

Allows interrupter modules to send interrupt requests to interrupt handlers.

Priority Resolution Function

The mechanism used by auto-negotiation to select the network connection type when more than one common network ability exists (100Base-TX, 100Base-T4, 10Base-T, and so on). The priority resolution table defines the relative hierarchy of connection types from the highest performance to the lowest performance.

Protocol

A set of rules and conventions that govern the exchange of information between communicating parties.

read cycle

Used to transfer 1, 2, 3, or 4 bytes from a slave to a master.

read-modify-write cycle

Used to both read from and write to a slave location without permitting any other master to access that location. Useful in multiprocessing systems.

Renegotiation

Restart of the auto-negotiation function caused by a connectivity change or user interaction.

Routing Table

A table containing information about the routes to nodes on other LANs. The connections which make up a route are made through gateways. When additional gateways are added, or when network addresses change, the routing table must be updated. Each node has a routing table to enable it to determine the routes to nodes on other LANs.

Slave

Detects DTB cycles initiated by a master.

slot

A position where a board can be inserted in a VMEbus backplane.

SNMP (Simple Network Management Protocol)

A high-level, standards-based protocol for network management, usually used in TCP/IP networks. An SNMP monitor controls and measures the activities of SNMP agents that are embedded in nodes and network devices on the network. SNMP relies on Management Information Bases (MIBs) embedded in the network resources to monitor and control the network.

SYSFAIL (System Fail)

Indicates that a failure has occurred in the system. Can be generated by any board on the VMEbus.

SYSRESET (System Reset)

Causes boards in slots to be reset.

system controller board

A board which resides in slot 1 of a VMEbus backplane.

TCP/IP (Transmission Control Protocol/Internet Protocol)

A set of communications protocols that define how different types of computers talk to each other. It is the standard architecture for internetworking multiple organizations, and the common link that ties the huge Internet together.

Technology Ability Field

An 8-bit field in the auto-negotiation Link Code Word that is used to indicate Local Device support for 10Base-T, 100Base-TX, 100Base-T4, and/or Full Duplex.

TP-PMD (Twisted-Pair, Physical Media Dependent)

The 100 Mbps FDDI standard as implemented on UTP cable.

utilities

These include a system reset line, a system fail line, and an AC fail line.

VME (Versa Module Eurocard)

VMEbus backplane

A printed circuit board (PCB) with 96-pin connectors and signal paths that bus the connector pins.

write cycle

Used to transfer 1, 2, 3, or 4 bytes from a master to a slave.

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